8088/86 Processor Timing

Dan Kohn
Instructor
University of Southern Mississippi

System Clock

section 8.6

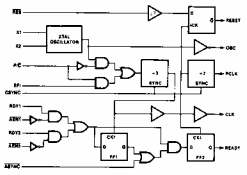
8088

- Two Speeds available
  - 5MHz (8088)
  - 8MHz (8088-2)

8086

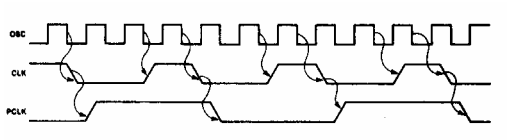
- Three Speeds Available
  - 5MHz (8086)
  - 8MHz (8086-2)
  - 10MHz (8086-1

8284
Clock Generator IC



- Divide by 3 (crystal freq / 3 = clock out)
  - 24MHz crystal -> 8 MHz at CLK output
- Duty Cycle on CLK is 33.3%
- Generates 2 additional clocks for peripheral IC's

Clock (cont)



Bus Cycle

section 8.7

- Defines the basic operation that a microprocessor performs to communicate with external devices.
- For the 8088/86 these consist of
  - 4 clock periods
  - T1, T2, T3 and T4
  - Additional Idle and Wait States can also exists

Timer States

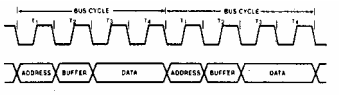
- T1
  - Address placed on bus
  - ALE active
- T2
  - Change direction of Data bus for READ instructions
- T3-4
  - Data transfer occurs

Wait and Idle States

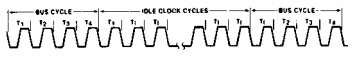
- Idle State
  - No bus activity required
  - 1 clock cycle
  - Occurs when instruction queue is full or the MPU does not need to read/write to memory
- Wait State
  - Triggered by events external to MPU
  - Buffer full will trigger a wait state
  - Triggered by READY pin
  - Inserted between T3 and T4

Wait and Idle

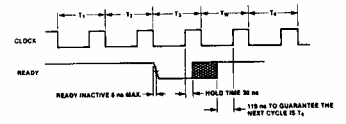
Normal Bus cycle



Idle Cycles

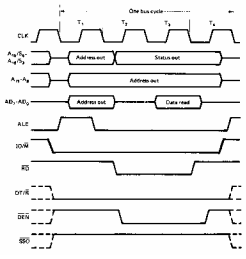


Wait state



Read Memory Cycle

Section 8.1

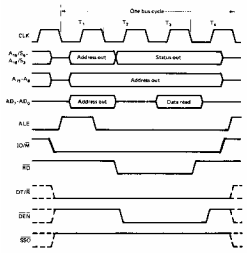


T1

- Output 20 bit address on A0-A19
- ALE goes active at same time
- Latching of the multiplexed address (AD0-AD7) occurs on Falling edge of ALE
- IO/M and DT/R are set to 0 indicating memory read is in progress

Read Memory Cycle

(cont)



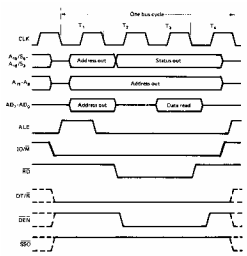
T2

- A16-A19 output Status bits S3-S6
- AD0-AD7 put in HIGH Z
- A8-A15 are maintained

- T2+
  - RD is set low (indicating a read operation)
  - DEN is set low (enable external circuitry to allow data to move from memory to the processor)

Read Memory Cycle

(cont)

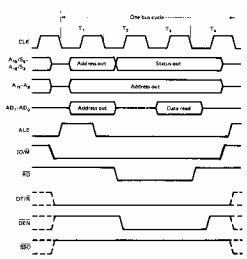


T3

- Data read

Read Memory Cycle

(cont)

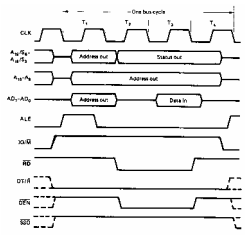


T4

- RD goes high
- DEN goes to inactive state
- Read cycle ends

Read Input Cycle

Section 8.18 (partial)



Read Input is similar to the Read Memory cycle except the IO/M line does not go low in T1 (indicating it is a IO function, not memory)